DCB Operation Manual

UMD LHCb Group

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Contents

1 System Introduction

1.1 Caution before handling a DCB: ESD, backplane connector

Electrostatic discharge, ESD, can easily damage DCBs. Make sure to **ground yourself when handling a DCB** with a wriststrap or a grounded conductive mat. Additionally, before plugging a DCB into a backplane, you must verify the backplane connector on the DCB is free of debris. If it is not, clean it carefully.

1.2 DCB purpose

The Data and Control Board (DCB) is part of the readout electronics for the Upstream Tracker (UT) detector at LHCb. The signals from the silicon sensors are read out by the following chain

$$\text{Sensor} \xrightarrow{\text{analog}} \text{ASIC} \xrightarrow{\text{digital}} \text{Hybrid} \rightarrow \text{Flex cables} \rightarrow \text{Backplane} \rightarrow \textbf{DCB} \xrightarrow{\text{optical}} \text{DAQ}.$$

This chain is illustrated in Fig. 1.

The backplanes and DCBs form the so-called PEPI electronics, and are housed in 24 crates located directly above and below the UT staves subject to a total ionization dose (TID) of about 100 krad over 10 years. Each crate contains one backplane and up to 12 DCBs reading two to six half staves. The pulses generated by the silicon sensors are shaped, digitized, and zero-suppressed by the 128-channel front-end SALT ASICs. These signals are then transmitted on 320 Mbps e-links via stave and pigtail flex cables to the PEPI boards. Up to 12 pigtail cables are connected to each backplane, which then routes the data to the DCBs with the goal of balancing the load carried by each board. Finally, the DCBs transmit these data to the central DAQ via 4.8 Gbps optical links. Additionally, the DCBs are responsible for the distribution of fast timing and slow control signals as well as the distribution of the low voltage power to the FE ASICs. Low speed I^2C buses are used for configuration and status monitoring.

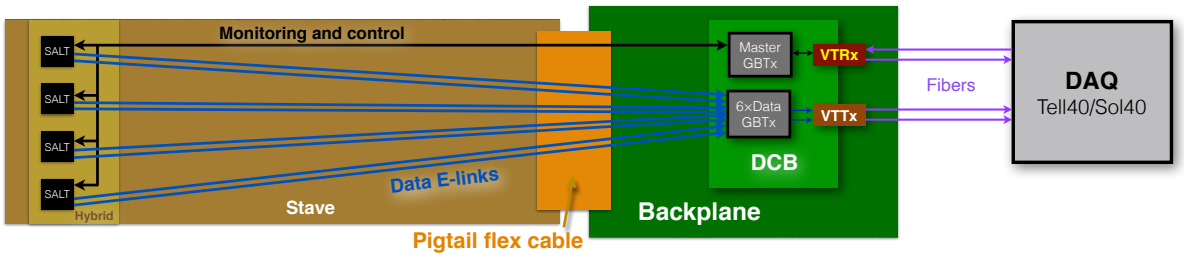

Figure 1: Schematic of the UT readout chain.

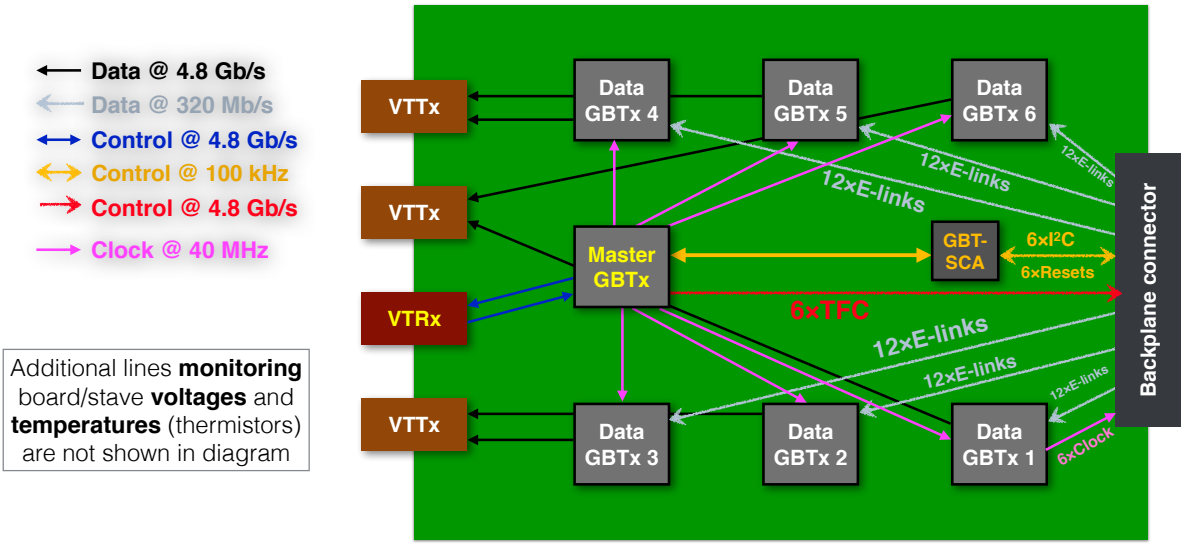

Figure 2: Distribution of the data and control signals in the DCB.

1.3 Description of the main components

Figure 2 shows the main components in a DCB as well as the distribution of the data and control signals. The main components and quantity in each DCB are

- **1 master GBTx**: it receives the machine clock from the counting room via VTRx optical link, and transmits clocks to the data GBTxs and GBT-SCA. It also transmits TFC (control signals) to the SALTs.
- **1 GBT-SCA**: it receives ECS information from the master GBTx and transmits it to the data GBTxs and SALTs. It also monitors temperature of the DCB and hybrids.
- **6 data GBTxs**: they serialize up to twelve 320 Mbps e-links into a single 4.8 Gbps line to transmit optically via VTTxs to the central DAQ. Data GBTx 1 (DC0) also transmits the reference clocks to the SALT ASICs.
- **1 Versatile Link Transceiver (VTRx)**: optical transceiver with one receiver link and one transmitter link that provides the communication with the master GBTx.
- **Up to 3 Versatile Link Transmitters (VTTx)**: optical transceiver with two transmitter links that converts the electrical 5.1 GHz signals from the data GBTxs into optical signals.

Note that while the optical transmission of the data occurs at 4.8 Gbps, the speed of the optical lines is 5.1 GHz to account for the protocol overhead.

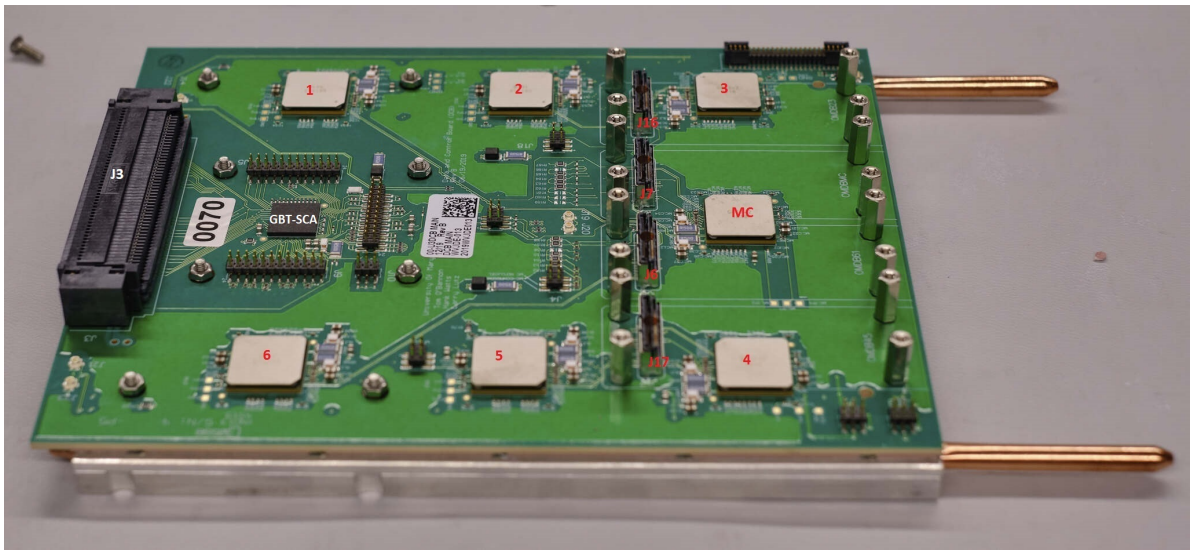

Figure 3: Major components of DCB. Data GBTxs are number 1-6 and MC is the master GBTx. J3 is the backplane connector, J6, J7, J16, J17 are the optical mezzanine connectors.

2 Physical System

2.1 Major DCB components

In addition to the CERN GBT chip set the board also uses 1 Samtec SEAF-50-01-L-08-2-RA-GP-K-TR connector (J3) to plug in to the backplane and 4 Samtec LSHM-130-06.0-L-DV-A-S-K connectors (J6, J7, J16, J17) to plug in the optical mezzanines. Their location on the board is shown in Figure 3.

2.2 DCB assembly

A link to instructions with additional detail can be found in Appendix A.

- Visually inspect the DCB.
- Place the thermal gap filler on the flat side of the baseplate and heat pipe assembly.
- Screw the DCB to the baseplate, using 16 M2.5 countersunk screws (McMaster-Carr 91430A081) and 8 M3 countersunk screws (McMaster-Carr 91430A120), with matching kapton washers (Seastrom 5611-130-5 and 5611-33-5), hex nuts (Bolt Depot 7363), and standoffs (Assman V6516D). The screws go on the baseplate side and washers and nuts on the DCB side, with the M2.5 screws at the optical mezzanine side of the board.
- Hand tighten in an x pattern, being careful not to scratch the board by twisting the nuts.
- Verify that the board ground is isolated from the baseplate.
- Apply jumpers according to the configuration shown in Figure 4.

- Insert VTTx/VTRx to optical mezzanine boards, be careful to push them all the way in. New VTTx/VTRx will need to have the raised screw thread carefully removed with wire cutters to sit flush with the board. Screw in with two M1.4 screws and washers (McMaster-Carr 91800A030 and 93475A179).
- Connect mezzanines to DCB and fix it with screws into the stand-offs.

2.3 Jumper configuration

The DCB is configured with 2mm jumpers, for example Harwin M22-1920005. The jumper configuration is shown in Figure 4. The headers here are described from the top to the bottom of the board, where pin 1 is in the top left marked with a dot and pin 2 corresponds to the top right pin:

- J13: Pin 1-2 are 1V5. Pins 5-6 are 3V3. Pins 3-4 are the Data GBTx efuse power. Both should be connected to 1V5 during normal operation.
- J2: Pin 1-2 are 1V5. Pins 5-6 are 3V3. Pins 3 and 4 are the SCA and MC efuse power. Both should be connected to 1V5 during normal operation. MC efuse should be connected to 3V3 for fusing.
- J4: Pin 1 is MC_CONFIGSELECT. When pulled up (unjumped) the Master GBTx can be configured through external I2C. When pulled down (jumped to pin 2) the Master GBTx can be configured through the IC field of the optical link. Pins 1 and 2 should be jumped during normal operation and unjumped during fusing.
  Pin 3 is MC_REFCLKSEL. When pulled up (unjumped) the Master GBTx relies on REFCLKP/N for its reference clock. When pulled down the Master GBTx relies on its own XPLL for its reference clock. This should be the mode for normal operation. Pins 5 and 6 are grounded.
- J12: Pin 1 is EC_RESET_GPIO_6 (GBT-SCA GPIO pin) and should be jumped to Pin 2, which is DC_RESETB. This ensures that the master GBTx can reset the data GBTxs. Pin 3 is EC_HYB_i2C_SCL_6 (GBT-SCA I2C clock output) and should be jumped to Pin 4, which is DC_I2C_SCL (Data GBTx I2C clock input). Pin 5 is EC_HYB_i2C_SDA_6 (GBT-SCA I2C data output) and should be jumped to Pin 6, which is DC_I2C_SDA (Data GBTx I2C data input). Connecting these I2C clock and data lines allows the GBT-SCA to communicate with the data GBTxs via I2C.
- J10: Pin 1 is SCA_AUXPORT_SDA, Pin 2 is SCA_AUXPORT_SCL. These pins are not used. Pins 3 and 5 are ground. Pin 3 should be jumped to Pin 4 (SCA_AUXPORT_TESTEN) and 5 to 6 (SCA_LINK_AUX_DISABLE). This disables auxiliary test ports for normal operation.

2.4 Monitoring pins

The full list of pins can be found in the DCB and optical mezzanine schematics linked in Section A. Only critical or commonly used pins are listed.

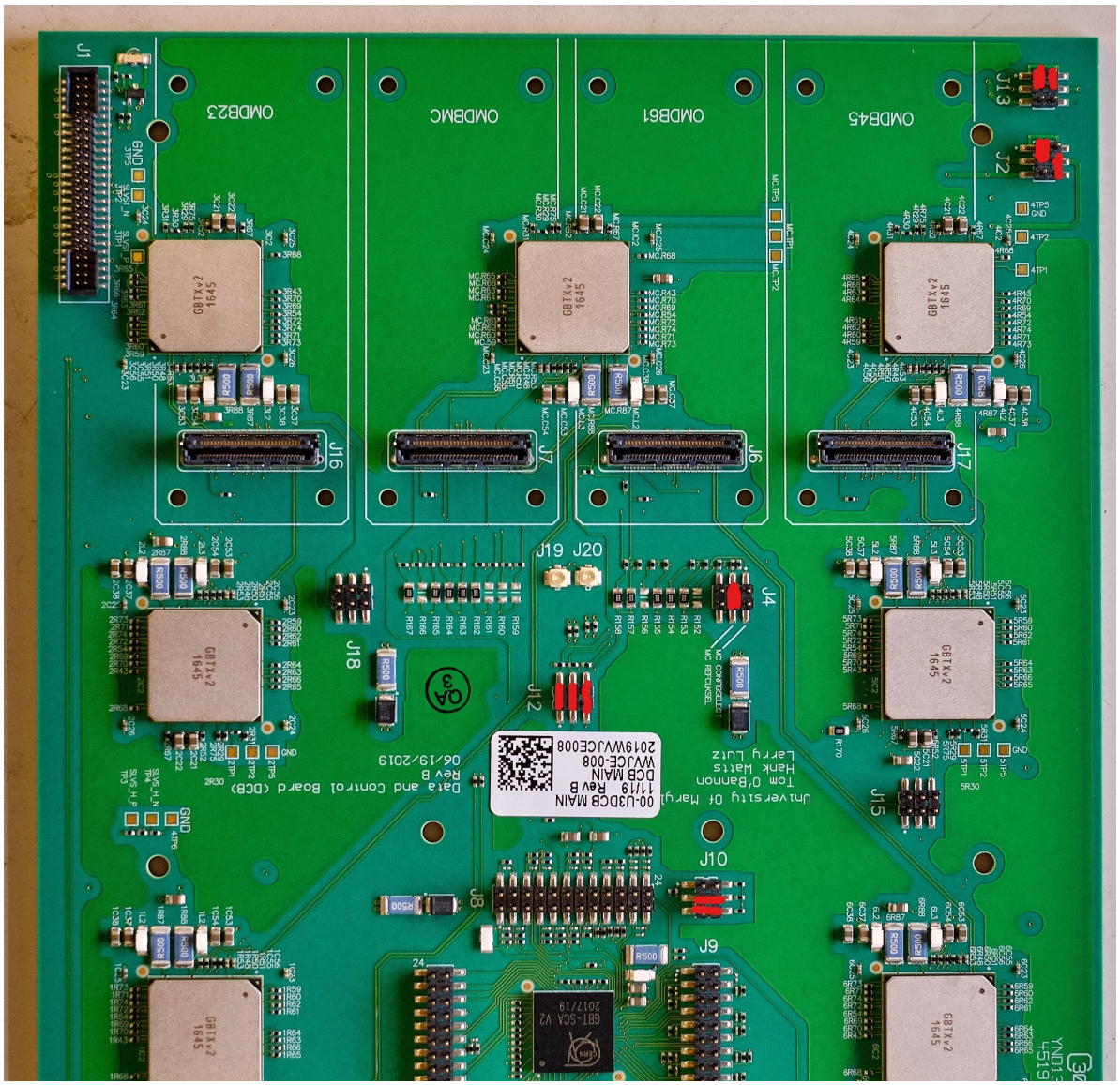

Figure 4: Jumpers for DCB configuration. Note that J2 is before fusing and during normal operation should be jumped the same way as J13. Similarly, J4 pins 1 and 2 should be jumped during normal operation.

Name	Pin	Description
GND	1	One of many ground pins
TX_RDY(A, B)	36, 6	Asserted when GBTx is ready for operation
TXDATAVALID(A)	38	When asserted transmitted frame contains data header
VCCT1	40	VTTx power (2V5)

Table 1: Critical pins of Data GBTx optical mezzanine J3 connector. A applies to GBTx 1, 3, 4 and B applies to GBTx 2, 5, 6. Can be accessed by connecting a FFC and breakout board, for example Assmann AFFC-050-40-153-11 and Newhaven Display NHD-FFC40.

Name	Pin	Description
MC_TX_RDY	36	Asserted when GBTx is ready for operation
MC_RX_RDY	37	Asserted when GBTx is ready for operation
MC_TXDATAVALID	38	When asserted transmitted frame contains data header
MC_RX_DATVAL	39	Asserted when received frame contains data header
MC_I2C_SDA	8	I2C data line for Master Gbtx
MC_I2C_SCL	10	I2C clock line for Master Gbtx
MC_RESETB	6	When asserted Master GBTx is held in reset

Table 2: Critical pins of Master GBTx optical mezzanine J3 connector. Can be accessed by connecting a FFC and breakout board, for example Assmann AFFC-050-40-153-11 and Newhaven Display NHD-FFC40.

3 Communication Interfaces

3.1 Data frame

GBTxs communicate with the counting room via data frames. Details of these frames can be found in the GBTx manual. Data GBTxs are operated in widebus mode, transmitting data at the maximum rate without error protection. The Master GBTx operates in normal mode with error protection. The frame includes data transmitted from the detector, and EC/IC fields for slow control of the detector.

3.2 I2C

Configuration registers of both Master and Data GBTx can be read and written via I2C. Directions for programming the GBTxs can be found in Yipeng and Mark's documentation.

The Master GBTx I2C can be accessed through pins 8(SDA) and 10(SCL) of the optical mezzanine connector (J3). In order to communicate this way the jumper on J4 pins 1-2 must be removed. The I2C is pulled up to 1.5V through 1k ohm resistors. The I2C address of the Master GBTx is 7.

The Data GBTx I2C can be accessed through pins 4(SCL) and 6(SDA) of J12, which are normally jumped to the GBT-SCA I2C port 6. The I2C is pulled up to 1.5V through 1k ohm resistors. The I2C address of each Data GBTx matches its number. Address 0 will address all Data GBTxs.

The I2C registers of the VTT/Rx GBLD chips can be accessed through the Master GBTx. Directions for programming them can be found in section 6 of the GBTx manual (or Mark and Yipeng's documentation).

Name	Connector	Description
MC_EFUSEPROGPULSE	Mez. J5	Pulsed to fuse Master GBTx
MC_RCLK_IN_(P, N)	J20, J19	Reference clock input for Master GBTx

Table 3: Critical u.Fl connectors for monitoring of DCBs

3.3 ADC

ADCs (analog to digital converters) can be read out through the DAQ system to verify the power and, for the ones attached to thermistors, monitor temperatures on the DCB itself and the stave.

ADC channels 24 and 25 measure the voltage of the 2v5 and 1v5 rails respectively. Each channel readout is the rail voltage divided by three.

ADC channel 0 measures the voltage across an NB-PTCO-330 thermistor located on the DCB. The resistance of the thermistor can be computed as $R_v = \left(\frac{V_0 - V_v}{R_1 V_v} - \frac{1}{R_2}\right)^{-1}$ where $R_1 = 1.3k\Omega, R_2 = 2k\Omega, V_0 = 1.5V$. The temperature in C can then be determined from $R_v = R_0 \cdot (1 + aT + bT^2)$ where $R_0 = 1k\Omega, a = 3.9083 \cdot 10^{-3}, b = -5.775 \cdot 10^{-7}$.

ADC channels 1, 16, 17, and 18 measure the voltage across TDK B57471V2472J062 thermistors located on the optical mezzanines 4-5, 2-3, 6-1, and master, respectively. In order to read out these channels, first enable the $100\mu A$ SCA current source, then measure the voltage across a mezzanine thermistor to get the corresponding thermistor resistance R_T. The temperature corresponding to this value can then be found in Table 4.

Temperature (Celsius)	R_T/R_{25}
5.0	2.7994
10.0	2.1406
15.0	1.6492
20.0	1.2798
25.0	1.0
30.0	0.78663
35.0	0.62277
40.0	0.4961
45.0	0.39757
50.0	0.32044
55.0	0.2597
60.0	0.21161
100.0	0.048769
150.0	0.011033

Table 4: Mezzanine thermistor resistances and temperatures, where $R_{25} = 4.7k\Omega$

ADC channels 2-7 can be connected to thermistors located on the detector hybrids (depending on position in the backplane).

3.4 GPIO

The GPIO lines are used exclusively to reset data GBTxs and SALTs. A low GPIO line holds the chip in reset, while high allows for normal function. Lines 0-5 can be connected to SALTs (depending on position in the backplane) while line 6 is connected to the data GBTxs.

3.5 e-link

The data GBTx e-links are connected to the detector to read out data. Between 6 and 12 e-links of each data GBTx are connected depending on the position in the backplane. The master GBTx e-links are not used.

4 Functionality Tests

A link to a full description of quality assurance tests performed can be found in Section A. In the future a link will be included to directions for Mark and Yipeng's MiniDAQ panels.

- VTRx functionality and Master GBTx response through the optical fibers can be checked by reading and modifying register 28 of the Master GBTx. Operational state can be confirmed by reading register 431.
- GBT-SCA response can be checked by reading and modifying any register of the GBT-SCA.
- Data GBTx response can be checked by programming the chip from the config file. Operational state can be confirmed by reading register 431.
- Data GBTx and VTTx functionality can be checked by configuring the Data GBTxs to generate PRBS data (register 28 = 03).
- Data GBTx connection to the detector can be tested by configuring the SALTs to generate PRBS data.
- TFC distribution can be tested by configuring the SALTs to loop back TFC and inspecting it visually.
- GPIO can be tested by pulling pins low to reset the connected data GBTx/SALT and verifying that it cannot be programmed.
- ADC can be tested by reading it and comparing to the expected voltage or temperature (see Section 3.3).

5 Normal Operation

5.1 Installation in the PEPI

- Make sure you are grounded.
- Inspect the backplane connector for damage or debris.
- Slide the DCB into the card guide, making sure it is oriented so that the connector will plug in to the backplane.
- Once the connector is engaged with the guideposts, hold on to both heat pipes and press firmly to plug in. The connector does not always click, but should not come out if you pull gently on the heat pipes.
- Plug in the optical fibers.
- To uninstall, first press the latch to disengage the optical fibers and disconnect them. Then pull firmly on the heat pipes until the connector disengages.

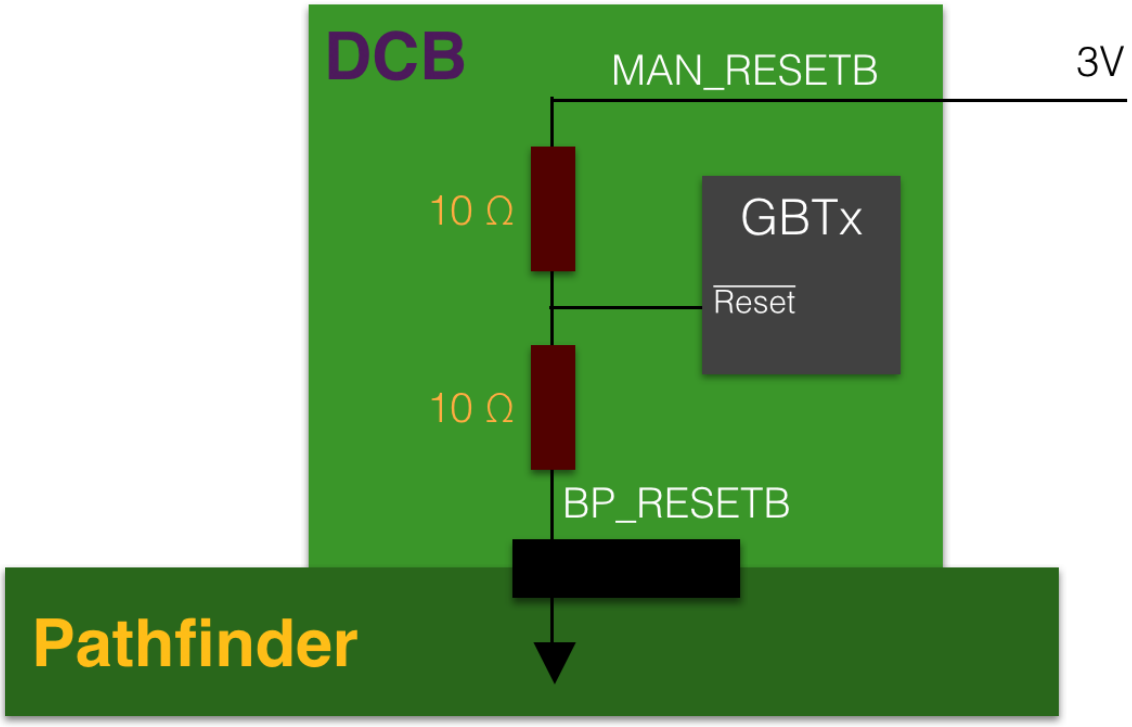

Figure 5: Schematic of the 3V pull-up needed for operations with the Pathfinder at CERN.

5.2 Operation

By default the Master GBTx is fused and will come up in the operating state. The Data GBTxs need to be programmed with their configuration files (Section A). Clock phases may need to be adjusted, see Mark's documentation if so. If VTTxs are in error the bias current will need to be adjusted (See GBTx and GBLD manuals). Once the data GBTxs are configured the DCB can operate normally.

5.2.1 CERN operation with pathfinder

At CERN the DCBs will be tested using a Pathfinder instead of the backplane which will be used in the final system. In the Pathfinder the RESET_B pin is grounded and therefore the DCB is held in reset. An external 3V pull-up is needed as shown schematically in Figure 5, which can be done using a FFC breakout board connected to the optical mezzanine. The detailed implementation depends on the FFC cable and the corresponding FFC breakout board, **it is crucial to understand the FFC cable configuration before connecting it as otherwise the 3V can damage the DCB if it is send to the wrong pin.** The actual setup used at CERN can be found in the following links: `https://umd-lhcb.github.io/ut-hw-doc/dcb/dcb_prod_with_pathfinder/dcb_prod_with_pathfinder/`, `https://umd-lhcb.github.io/ut-hw-doc/cern/cern_qa/cern_qa/`.

6 Troubleshooting

6.1 Common QA errors and fixes

- Any problem when using FFCs (e.g. for pull-up with pathfinder backplane): Inspect FFCs for damage and carefully reseat, wiggling to ensure both corners are flush with the connector. Also inspect the kapton tape which is used for shielding of the FFC cables and replace it if needed. This is by far the most common source of DCB problems.
- No response from master: check MiniDAQ, check power, check optical fiber polarity, reset power, check jumpers.
- No response from SCA: reset SCA, check jumpers.
- No response or bad PRBS from data GBTx: reset data GBTx, check data GBTx state, probe J12 to check I2C communication, reset power, check jumpers.
- No response or bad PRBS from SALT: reset SALT, reset power, check DCB connection to backplane, check pigtail connection.

6.2 Problems that have required rework

- PRBS errors from data GTBx: data GBTx or corresponding LSHM connector requires replacement.
- PRBS errors from SALT but not data GBTx: data GBTx or backplane connector requires replacement.
- Problems communicating with SALT: GBT-SCA or backplane connector requires replacement.
- Master GBTx fusing fails: replace master GBTx.
- Problems communicating with data GBTx: GBT-SCA or data GBTx requires replacement.

A Links to additional DCB documentation

- DCB assembly: `https://umd-lhcb.github.io/ut-hw-doc/dcb/dcb_assembly/dcb_assembly/`
- DCB fusing and testing: `https://umd-lhcb.github.io/ut-hw-doc/dcb/dcb_qa/dcb_qa/`
- DCB master configuration: `https://github.com/umd-lhcb/nanoDAQ/blob/master/gbtx_config/master.txt` **To do: this should be put in EDMS**
- DCB data configuration: `https://github.com/umd-lhcb/nanoDAQ/blob/master/gbtx_config/slave-Tx-wrong_termination.txt` **To do: this should be put in EDMS**
- DCB schematic: `https://raw.githubusercontent.com/umd-lhcb/electronic-projects/master/dcb/schematic_dcb.pdf`
- DCB optical mezzanine schematic: `https://raw.githubusercontent.com/umd-lhcb/electronic-projects/master/dcb/schematic_dcb_opt_mezz.pdf`
- GBTx manual: `https://espace.cern.ch/GBT-Project/GBTX/Manuals/gbtxManual.pdf`
- GBLD manual: `https://readthedocs.web.cern.ch/ate/files/113213790/113213794/1/1556903336000/GBLD_manual-June2015.pdf`

B DCB fusing procedure

- Check that all jumpers are in the pre-fusing position (Figure 4).
- Connect a FFC and breakout board (for example Assmann AFFC-050-40-153-11 and Newhaven Display NHD-FFC40) to the VTRx optical mezzanine.
- Connect pin 2 of the USB-I2C adapter (`https://espace.cern.ch/GBT-Project/VLDB/Control/Forms/AllItems.aspx`) to the J5 optical mezzanine u.Fl (this requires making a specialized cable).
- Connect pins 3, 5, and 7 of the USB-I2C adapter to pins 31, 32, and 34 of the FFC breakout board.
- Supply 3v3 power through the test connector J1 (this requires a board-mounted connector) and power on both 3v3 and 1v5.
- Use the GBT programmer (`https://gitlab.cern.ch/gbtproj/gbtxprogrammer`) to write and verify the configuration file.
- Check the "enable Fusing" and "fuse updateConfig" boxes of the fusing panel and fuse the DCB.
- Adjust jumpers according to Section 2.3 and verify the fusing.