## LVR final QA checklist

1. Put on wrist strap, take LVR from box, set all switches to values in table

	CCMs	Is FPGA side			
	SW1	SW3	SW2	SW5	
All	0001	1111	1111	0000	

	CCMs		
	SW6[ABCD]		
1.2V	1010		
1.5V	1100		
2.5V	1000		

	FPGA
	SW4
Α	0000
MS	1111
MSA	1100

- 2. Slide LVR in frame, tighten wedge locks
- 3. Measure GND-Earth (**TP7-lugs**) separation  $> 25k\Omega$  in both directions
- 4. Connect input BB, Rpi monitor, and turn on **PS to 6V** 
  - [If fw not 2.06] Connect JTAG dongle, program with **fw tag 2.06**
- 5. **Adjust P1, P2, and P5** if the base voltages are not as expected (Vin\_FPGA\_1V5=1.5 V, Vin FPGA 3V3=3.3 V, V OPAMP RAIL=5.5 V)
- 6. Request WORD2 to confirm fw version is 2.06 and turn all channels ON with Rpi Butler
- 7. **Adjust the CCM potentiometers** if V\_SENSE\_MONi voltages are not 1.25V, 1.52V, or 2.51V
- 8. Check UVL turns all channels OFF with input voltage 4.3V (12A), 4.8V (15MS), 5.3V (25A)
  - Set input voltage back to 6V when you've checked
- 9. Change **SW1** to 0011 (or 1111), check over-temperature turns **channels off, LD7 LED turns on**
- 10. Set channels to READY, adjust P3-P4 for V\_SENSE to be 110-190 mV (better 120-140 mV)
- 11. Turn channels OFF, connect MPSS cable and RJ45 sense lines to each output
  - 1. Scope to Single, "Ripple ON" and see smooth turn on, plateaus above desired voltages
  - 2. Check voltage drop across R75 and R91 is same
  - 3. **Disconnect sense lines**, see them match non-sensed channels
- 12. **Turn off PS, remove CCM8, move J22 jumpers** to right (connecting pins 4&6 and pins 3&5)
- 13. **Set a valid 'sub type'** in DB, remove CCMs as necessary. For each removed CCM, one of the switches on SW3/SW2 (and SW4 if slave) must be set to OFF
- 14. **Update the database**, and you are done!

8ch, FF	7ch, 7F	7ch, BF	6ch, 5F	6ch, BB
INPUT	INPUT	INPUT	INPUT	INPUT
5 CCM CCM 4	5 CCM CCM 4	5 CCM CCM 4	5 CCM CCM 4	5 CCM CCM 4
6 CCM CCM 3	6 CCM CCM 3	6 CCM CCM 3	6 open CCM 3	6 CCM open 3
7 CCM CCM 2	7 CCM CCM 2	7 open CCM 2	7 CCM CCM 2	7 open CCM 2
8 CCM CCM 1	8 open CCM 1	8 CCM CCM 1	8 open CCM 1	8 CCM CCM 1
OUTPUT OUTPUT	OUTPUT OUTPUT	OUTPUT OUTPUT	OUTPUT OUTPUT	OUTPUT OUTPUT
5ch, D9	4ch, 0F	5ch, 1F	4ch, CC	6ch, F6
INPUT	INPUT	INPUT	INPUT	INPUT
5 CCM CCM 4	5 open CCM 4	5 CCM CCM 4	5 open CCM 4	5 CCM open 4
6 <mark>open open</mark> 3	6 open CCM 3	6 open CCM 3	6 open CCM 3	6 CCM CCM 3
7 CCM open 2	7 open CCM 2	7 open CCM 2	7 CCM open 2	7 CCM CCM 2
8 CCM CCM 1	8 open CCM 1	8 open CCM 1	8 CCM open 1	8 CCM open 1
OUTPUT OUTPUT	OUTPUT OUTPUT	OUTPUT OUTPUT	OUTPUT OUTPUT	OUTPUT OUTPUT
5ch, F2	4ch, F0			
INPUT	INPUT			
5 CCM open 4	5 CCM open 4	12M 12S 12A		
6 CCM open 3	6 CCM open 3	15M 15S 25A		
7 CCM CCM 2	7 CCM open 2			
8 CCM open 1	8 CCM open 1			
OUTPUT OUTPUT	OUTPUT OUTPUT			